WHAT IS CLAIMED IS:

1. A circuit substrate comprising:

a plurality of terminals formed on a substrate; and

one or more resistances formed between said terminals adjacent one to another;

wherein said plurality of terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminals connected to digital signal lines for supplying digital signals;

and wherein said resistance which has at least one end thereof connected to said analog terminal, has a resistance value greater than said resistance connected between said digital terminals.

2. A circuit substrate comprising:

a plurality of terminals formed on a substrate; and

one or more resistances formed between said terminals adjacent one to another;

wherein said plurality of terminals include first terminals connected to data lines for supplying data signals, and second terminals connected to control lines for supplying control signals;

and wherein said resistance which has at least one end thereof connected to said first terminal, has a resistance value greater than said resistance connected between said second terminals adjacent one to another.

3. A circuit substrate comprising:

a common electrode line formed on the perimeter of a substrate;

a plurality of terminals formed on said substrate; and

one or more resistances formed between said terminals and said common electrode line;

wherein said plurality of terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminals connected to digital signal lines for supplying digital signals;

and wherein said resistance connected to said analog terminal has a resistance value greater than said resistance connected to said digital terminal.

4. A circuit substrate comprising:

a common electrode line formed on the perimeter of a substrate;

a plurality of terminals formed of said substrate;

one or more first resistances formed between said terminals adjacent one to another; and

one or more second resistances formed between said terminals and said common electrode line.

5. A circuit substrate according to Claim 4, wherein said terminal is connected to both said first resistance and said second resistance;

and wherein said first resistance has a resistance value greater than said second resistance.

6. A circuit substrate according to Claim 5, wherein said plurality of terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminal connected to digital signal lines for supplying digital signals;

and wherein both said first resistance and said second resistance which have at least one end thereof connected to said analog terminal, have resistance values greater than both said first resistance which is connected between said digital terminals, and said second resistance which is connected between said digital terminal and said common electrode line.

7. A circuit substrate according to Claim 1, further comprising:

electric power terminals connected to a power source; and

resistances formed between said electric power terminals and adjacent non-electric power terminals formed for purposes other than supplying power.

8. A circuit substrate according to Claim 7, wherein said resistance has a resistance value equal to or less than the resistance connected to other non-electric power terminals.

9. A circuit substrate comprising:

a common electrode line formed on the perimeter of a substrate;

data line terminals connected to data lines for supplying analog signals;

control signal terminals connected to control signal lines for supplying digital signals;

electric power terminals for supplying negative electric power or positive electric power;

first resistances connected between said terminals adjacent one to another; and

second resistances connected between said terminals.

10. A circuit substrate according to Claim 9, wherein, in the event that any of said terminals are connected to both said first resistance and said second resistance, said first resistance has a resistance value greater than said second resistance.

11. A circuit substrate according to Claim 10, wherein both said first resistance and said second resistance which have at least one end thereof connected to said data terminal, have resistance values greater than any of said first resistance connected between said control signal terminals, said first resistance connected between said control signal terminal and said electric power terminal, said second resistance connected between said control signal terminal and said common electrode line, and said second resistance connected between said electric power terminal and said common electrode line.

12. A circuit substrate according to Claim 11, wherein said resistances are formed of a semiconductor film.

13. A circuit substrate according to Claim 1, wherein said resistance includes a protection circuit configuration employing PN junction configurations with reverse polarity.

14. An electro-optical device including a circuit substrate according to Claim 1.

15. An electronic apparatus including an electro-optical device according to Claim 14.

16. A manufacturing method for a circuit substrate including a common electrode line on the perimeter thereof and a plurality of terminals on the inner side of said substrate from said common electrode line, comprising:

a step for forming one or more first resistance configurations on regions between said terminals adjacent one to another;

a step for forming one or more second resistance configurations on regions between said terminals and said common electrode line;

a step for forming said terminals which are electrically connected to a part of said first resistance configurations or/and said second resistance configurations; and

a step for forming said common electrode lines which are electrically connected to a part of said second resistance configurations.

17. A manufacturing method for a circuit substrate according to Claim 16, wherein said first resistance configurations and said second resistance configurations are formed so that said first resistance configuration has a resistance value greater than said second resistance configuration.